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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/749,570	12/31/2003	Mikko Waltari	109822-98	8972

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EXAMINER	
WAMSLEY, PATRICK G	

ART UNIT	PAPER NUMBER
2819	

DATE MAILED: 10/17/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/749,570	WALTARI, MIKKO	
	Examiner	Art Unit	
	Patrick G. Wamsley	2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 August 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *3,13 and 16* is/are allowed.

6)☒ Claim(s) *1,2,5-12,14,15 and 18-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *31 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

Applicant's arguments with respect to claims 1-3, 5-16, 18-21 have been considered but are moot in view of the new grounds of rejection.

Double Patenting

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

Claims 1, 7-11, and 18-20 are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1, 10-14, and 17-19 of copending Application No. 10/749,571 to Waltari, hereafter Waltari. Although the conflicting claims are not identical, they are not patentably distinct from each other because of the reasons listed below.

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

For independent claim 1, claim 1 of Waltari also recites an algorithmic analog-to-digital converter, hereafter ADC, comprising a sample-and-hold circuit and an ADC processing unit. While this application describes the use of a single internal ADC clock, Waltari provides a single operational amplifier. These limitations are actually obvious in view of each other, because the use of a single amplifier would necessitate the use of a single clock.

For independent claim 11, claim 14 of Waltari also recites a method comprising the steps of sampling and holding an input signal and generating bits. While this application describes the use of two cycles of variable length, Waltari adds sets of bits to generate an output signal. The variable length limitation would have been obvious because Waltari needs two clock phases, one for applying a signal to switched capacitors and another for comparing their charges to reference voltages.

For independent claim 18, claim 17 of Waltari provides a method comprising the steps of sampling and holding an input signal, generating an ADC clock, generating new voltages, generating data bits, generating feedback signals, and generating output bits. This application differs from Waltari by reciting the use of a different length cycles for the ADC clock. However, it would have been obvious to use variable cycle lengths in Waltari, corresponding to sampling and comparison ADC operations.

Claim 7 corresponds to claim 10 in Waltari.

Claim 8 corresponds to claim 11 in Waltari.

Claim 9 corresponds to claim 12 in Waltari.

Claim 10 corresponds to claim 13 in Waltari.

Claim 19 corresponds to claim 18 in Waltari.

Claim 20 corresponds to claim 19 in Waltari.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the

invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 2, 5-12, 14-15, and 18-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over the Admitted Prior Art, hereafter APA, in view of U.S. Patent 6,909,393 to Atriss et al, hereafter Atriss.

APA discloses an algorithmic analog-to-digital converter [Page 2, ¶3], hereafter ADC, able to sample a continuous analog signal and quantize it into a set of discrete levels. Thus, APA discloses both a S/H function [sampling], and an ADC operation [quantization]. APA's algorithmic ADCs also comprise at least two single-bit processing units sharing a common operational amplifier [Page 3, ¶4]. Conventional algorithmic ADCs [Page 20, ¶76] have two MDACs operating in opposite phases - one generates a residue, while the other performs sampling. These MDACs inherently comprise switched capacitor circuits, which were also described as "typical" by applicant on page 9, ¶40. Such circuits inherently have feedback signals in the context of an ADC system, as the DAC itself serves as a feedback element.

As depicted in Fig. 4, Atriss provides an ADC clock signal occurring at a much greater frequency than a cycle rate for a sample / hold circuit. For claim 1, as shown in Fig. 6, Atriss permits sample / hold circuitry [82] to share a single amplifier [81] with an ADC processing unit [83]. At the time of the invention, it would have been obvious to one of ordinary skill in the art to have applied the teachings of Atriss to APA's algorithmic ADC. The motivation would have been to provide an ADC that operates at high clock rates [col. 1, lines 58-59].

As depicted in Fig. 4, Atriss provides an ADC clock signal occurring at a much greater frequency than a cycle rate for a sample / hold circuit. At the time of the invention, it would have been obvious to one of ordinary skill in the art to have applied the teachings of Atriss to APA's algorithmic ADC. The motivation would have been to provide an ADC that operates at high clock rates [col. 1, lines 58-59].

For claims 1, 11, 14, and 18, in the APA / Atriss combination, the ADC clock is at least twice as fast as the timing rate of the sample / hold circuit.

For claims 2, 12, 15, and 21, the APA / Atriss combination uses the number of clock cycles to determine the resolution of the generated digital word [col. 13, lines 1-2]. Shorter cycles can be used when less accuracy is needed.

For claim 5, Atriss, like APA, provides a multiplying digital to analog converter, hereafter MDAC, coupled to a sub-ADC stage. The sample / hold circuit is integrated with MDAC in the APA / Atriss combination.

For claims 6 and 19, in the combination, each clock signal comprises at least two phases, one for sampling [61: Fig. 4], and one for comparison [62: Fig. 4].

For claim 7-10, APA's algorithmic ADC, as modified by Altriss, can function in video encoder, video decoder, set top box, and an electronic appliance.

For claims 18 and 20, the APA / Altriss combination applies feedback signals to determine which reference voltages are applied to the switched capacitors.

Allowable Subject Matter

Claims 3, 13, and 16 are allowed.

The following is a statement of reasons for the indication of allowable subject matter: the references of record neither reveal nor render obvious the use of a delay locked loop, hereafter DLL, to generate an internal ADC clock having at least two cycles of different length.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. U.S. Patent 6,927,722 to Hong discloses switched capacitor circuits [SCCs] coupled to an operational amplifier [220]. U.S. Patent 6,608,504 to Fujimoto provides a sample-and-hold circuit for pipelined ADCs. U.S. Patent 6,570,519 to Yang uses switched capacitors [400] with an operational amplifier [306]. U.S. Patent 6,195,032 to Watson et al provides different clocks for MSB [90] and LSB [92] sub-stages. U.S. Patent 5,703,589 to Kalthoff et al links an operational amplifier [18] to a switched capacitor circuit [25].

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Patrick G. Wamsley whose telephone number is (571) 272-1814. The official facsimile number is (571) 273-8300. An alternate facsimile number, (571) 273-1814, should only be used for unofficial documents.

Patrick G. Wamsley
October 11, 2005